Notice of Allowability	Application No.	Applicant(s)	
	09/344,847	PANESAR, GAJINDER SINGH	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *October 19, 2004*.

2. ☒ The allowed claim(s) is/are *1-9*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

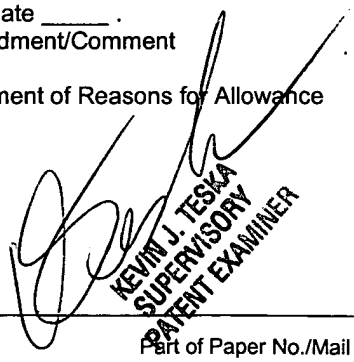
6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.



DETAILED ACTION

Introduction

1. This communication is in response to the Applicant's response filed on October 19, 2004. Claims 1-9 of the application are pending.

Drawings

2. The proposed correction to the drawing filed on October 19, 2004 is approved. In order to avoid abandonment of this application, corrected drawing is required in reply to the Office action. The correction will not be held in abeyance.

Reasons for Allowance

3. Claims 1-9 of the application are allowed over prior art of record.

4. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) an integrated circuit modeling system for automatic design of register sets and register based hardware devices such as ASIC; a particular function in the hardware of ASIC is activated by accessing the correct associated register; by reading or writing to the registers, the internal

fields in the register are externally accessed and programmed; the action of accessing the fields causes the hardware to be set in a particular manner and ultimately perform the desired associated function; a device may consist of hundreds of registers with multiple fields and so the development of hardware device is complicated; the system generates major design outputs from a single text based register specification file; the register specification source file contains all register information such as its offset, access permission, size, and field specifications; the system accesses the register specification source file and automatically generates behavior model register code and IC simulation code; (**Aleksic et al.**, U.S. Patent 5,995,736);

(2) a method of making an application specific hardware simulator for testing/debugging by simulation, the software of a plurality of input/output devices for embedded system; from the hardware specification including hardware architecture, memory map and register definition, a guidance is displayed to the user, enabling the user to input subsystem definition; the hardware specification and the subsystem definition table are related to each other to prepare the specification of system architecture; the system architecture is used with the simulator in a simulator library to generate test environment programs; the source program for the test environment is automatically generated by user selecting the testee section; (**Shimabukuro et al.**, U.S. Patent 5,557,774); and

(3) a coverification system and method for performing simulation, hardware acceleration and coverification of target system and external I/O devices; the hardware/software coverification occurs before fabrication of the design of the ASIC; one type of coverification tool uses the actual ASIC while another type uses an emulator; the target system and the external I/O

devices are modeled in the software; the time from initial design to a verified working ASIC chip is shortened; (**Lin et al.**, U.S. Patent 6,389,379).

4.1 Applicant's first set of claims consists of Claims 1-4.

Independent Claim 1 is directed to a method of operating a computer system to design an application specific processor (ASP). The claim identifies the uniquely distinct features of:

"generating for each peripheral an input file which defines the functional attributes of that peripheral in a high level language with an input data structure" and "entering the input file into the computer system and operating a modelling tool loaded on the computer system to generate from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table".

The closest prior art fails to teach or fairly suggest generating for each peripheral an input file which defines the functional attributes of that peripheral in a high level language with an input data structure and entering the input file into the computer system and operating a modelling tool loaded on the computer system to generate from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table, as claimed by the Applicant. Therefore, Claims 1-4 are deemed novel and allowable.

4.2 Applicant's second set of claims consists of Claims 5-7.

Independent Claim 5 is directed to a computer system which comprises a processor and a memory, the memory holding a program representing a modelling tool for use in designing an application specific processor (ASP). The claim identifies the uniquely distinct features of:

"an input means for receiving a plurality of input files, each input file defining the functional attributes of a peripheral for the ASP in a high level language within an input data structure" and "the processor being operable to execute the program representing the modelling tool to generate from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table".

The closest prior art fails to teach or fairly suggest an input means for receiving a plurality of input files, each input file defining the functional attributes of a peripheral for the ASP in a high level language within an input data structure and the processor being operable to execute the program representing the modelling tool to generate from the input file a register definition file by allocating specific elements of the input data structure to predefined sectors of a register definition table, as claimed by the Applicant. Therefore, Claims 5-7 are deemed novel and allowable.

4.3 Applicant's third set of claims consists of Claim 8.

Independent Claim 8 is directed to a computer program product stored on a computer readable medium and comprising software code portions operable when executed by a computer. The claim identifies the uniquely distinct features of:

"to read an input file which defines in an input data structure the functional attributes of a peripheral for an application specific processor in a high level language" and "to generate from that input file a register definition file, the software code portions including a code portion for allocating specific elements of the input data structure to predefined sectors of a register definition table for each of a plurality of registers".

The closest prior art fails to teach or fairly suggest to read an input file which defines in an input data structure the functional attributes of a peripheral for an application specific processor in a high level language, and to generate from that input file a register definition file, the software code portions including a code portion for allocating specific elements of the input data structure to predefined sectors of a register definition table for each of a plurality of registers, as claimed by the Applicant. Therefore, Claim 8 is deemed novel and allowable.

4.4 Applicant's fourth set of claims consists of Claim 9.

Independent Claim 9 is directed to a register definition file stored on a computer readable medium and comprising a plurality of register definition tables wherein the computer readable medium is loaded into a computer for simulating an Application Specific Processor. The claim identifies the uniquely distinct features of:

"each table including at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element, and each table further including the word location of the register within a memory map".

The closest prior art fails to teach or fairly suggest each table including at least predefined sectors for the bit location within a register of an element, the name of the element, the function of the element and the functional status of the element, and each table further including the word location of the register within a memory map, as claimed by the Applicant. Therefore, Claim 9 is deemed novel and allowable.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
January 3, 2005